PATENT AF/pw

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	10/726,638
Filing Date:	December 4, 2003
Appellants:	Ja-Hum KU et al.
Group Art Unit:	2812
Examiner:	Richard A. Booth
Title:	NICKEL ALLOY SALICIDE TRANSISTOR STRUCTURE AND METHOD FOR MANUFACTURING SAME
Attorney Docket:	2421-000030/US

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December 29, 2008

APPELLANTS' BRIEF ON APPEAL UNDER 37 C.F.R. § 41.37

Sir:

In accordance with the provisions of 37 C.F.R. § 41.37, Appellants submit the following Appeal Brief.

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I. REAL PARTY IN INTEREST

The real party in interest for the present application is Samsung Electronics Co., Ltd. An assignment of the rights associated with the present application was recorded with the United States Patent and Trademark Office on December 4, 2003 on reel/frame no. 014766/0714.

II. RELATED APPEALS AND INTERFERENCES

Co-pending Application No. 11/148,301, "NICKEL ALLOY SALICIDE TRANSISTOR STRUCTURE AND METHOD FOR MANUFACTURING SAME" under appeal as of October 7, 2008 is related to the present application in that both applications disclose similar subject matter.

III. STATUS OF CLAIMS

Claims 1-34 are pending in the current application. Claims 1 and 15 are in independent form. No claim amendments are being filed in conjunction with this request.

IV. STATUS OF AMENDMENTS

A Request for Reconsideration was filed in response to the July 3, 2008 Final Office Action, but included no claim amendments.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 recites "[a] method of forming a nickel silicide layer on an exposed silicon surface". This reads on the example embodiment on p. 12, par. [0041], of the original specification. Claim 1 additionally recites "depositing a nickel alloy layer on the exposed silicon surface, the nickel alloy including nickel and an alloying metal that constitutes no more than about 10 atomic percent of the nickel alloy". This reads on the example embodiment on p. 16, par. [0050] of the original specification. Claim 1 also recites "reacting the nickel alloy layer with the exposed silicon surface to form a nickel silicide layer having an upper layer and a lower layer". This reads on the example embodiment on pp. 15-16, par. [0049] of the original specification. Claim 1 further recites "wherein the alloying metal is preferentially segregated in the upper layer". This reads on the example embodiment on p. 17, par. [0053] of the original specification.

Independent claim 15 recites "[a] method of manufacturing a semiconductor device". This reads on the example embodiment on p. 9, par. [0032], of the original specification. Claim 15 additionally recites "defining an active region on a semiconductor substrate; [and] forming a gate electrode in the active region". This reads on the example embodiment on p. 9, par. [0033] of the original specification. Claim 15 also recites "exposing a silicon surface on the semiconductor substrate". This reads on the example embodiment on p. 11, par. [0038] of the original specification. Claim 15 further recites

"forming a nickel alloy layer on the semiconductor substrate, the nickel alloy including nickel and an alloying metal that constitutes no more than about 10 atomic percent of the nickel alloy". This reads on the example embodiment on p. 16, par. [0050] of the original specification. Claim 15 also recites "reacting a portion of the nickel alloy layer with the exposed silicon surface to form a nickel silicide region". This reads on the example embodiment on p. 10, par. [0035] of the original specification. Claim 15 additionally recites "removing an unreacted portion of nickel alloy layer from the semiconductor substrate". This reads on the example embodiment on p. 10, par. [0036] of the original specification. Claim 15 further recites "wherein the nickel silicide region includes an upper layer and a lower layer". This reads on the example embodiment on pp. 15-16, par. [0049] of the original specification. Claim 15 also recites "further wherein the alloying metal is preferentially segregated into the upper layer". This reads on the example embodiment on p. 17, par. [0053] of the original specification.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Review is requested for the rejections of (i) claims 1-4, 7-9, 15-18, 26, 28-29 and 31-34 under 35 U.S.C. § 102(e) as being anticipated by U.S. Publication No. 2005/0176247 (Cabral Jr. et al., hereinafter "Cabral"), (ii) claim 30 under 35 U.S.C. § 103(a) as being unpatentable over Cabral, (iii) claims 5-6, 10-14, 19-20 and 27 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Cabral Jr. et al. as applied to claims 1-4, 7-9, 15-18, 26, 28-29, and 31-34 above, and further in view of U.S. Patent No. 6,846,734 (Amos et al., hereinafter "Amos"), (iv) claims 21-25 under 35 U.S.C. § 103(a) as being unpatentable over Cabral Jr. et al. as applied to claims 1-4, 7-9, 15-18, 26, 28-29, and 31-34 above, and further in view of U.S. Patent No. 6,498,080 (Chittipeddi et al., hereinafter "Chittipeddi"). Appellants direct the Board's attention to the Response filed on September 3, 2008, which addresses the above rejections.

VII. ARGUMENT

Appellant respectfully requests that the Board reverse the final rejections of pending claims 1-34, because the pending claims are neither anticipated nor obvious over the cited art. The Examiner has rejected claims 1-4, 7-9, 15-18, 26, 28-29 and 31-34 under 35 U.S.C. § 102(e) as being anticipated by Cabral; rejected claim 30 under 35 U.S.C. § 103(a) as being unpatentable over Cabral; rejected claims 5-6, 10-14, 19-20 and 27 under 35 U.S.C. § 103(a) as being unpatentable over Cabral in view of Amos; rejected claims 21-25 under 35 U.S.C. § 103(a) as being unpatentable over Cabral in view of Chittipeddi. *See, e.g.*, Final Office Action dated July 3, 2008 ("Final OA"), p. 2.

With regard to independent claims 1 and 15, the Final OA states that it is inherent from the disclosure of Cabral that a nickel silicide layer has an upper layer and a lower layer, wherein the alloying metal is preferentially segregated in the upper layer. *See, e.g.*, Final OA, p. 2. Applicants respectfully submit that the Examiner has failed to meet the Examiner's burden of establishing a proper prima facie case of anticipation regarding claims 1-4, 7-9, 15-18, 26, 28-29 and 31.

1. Principles of Law

MPEP § 2112 states "the fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency

of that result or characteristic. *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993) (reversed rejection because inherency was based on what would result due to optimization of conditions, not what was necessarily present in the prior art); *In re Oelrich*, 666 F.2d 578, 581-82, 212 USPQ 323, 326 (CCPA 1981). Further, "in relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original).

2. Examiner Has Failed to Establish Inherency

Applicants respectfully submit that the Examiner does not provide the required objective evidence or cogent technical reasoning to support his conclusion of inherency.

Not only does the Examiner lack the required objective evidence to support his conclusion of inherency, Cabral actually discloses that the nickel alloy layer is a single layer, rather than a nickel silicide layer or region having an upper and lower layer as recited in independent claims 1 and 15.

As is clear from FIG. 2 of Cabral reproduced below, following formation of the Ni alloy layer, an annealing process step is performed which converts a portion of the metal alloy layer into a **non-agglomerated** Ni alloy monosilicide 1 atop a Si-containing material 10. *See* Cabral, paragraphs [0045] and [0049].

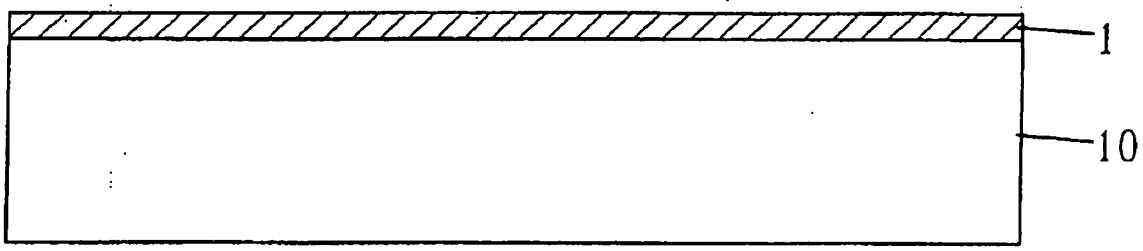

FIG. 2

Therefore, Applicants respectfully submit that Cabral does not teach or suggest reacting the nickel alloy layer with the exposed silicon surface to form a nickel silicide layer or region having an upper layer and a lower layer, wherein the alloying metal is preferentially segregated in the upper layer as recited in independent claims 1 and 15, but rather teaches a single non-agglomerated Ni alloy monosilicide layer.

Claims 2-14 and 16-34 are allowable at least for depending from an allowable base claim. Therefore, withdrawal of the rejection of claims 1-34 under either 35 U.S.C. § 102(e) or § 103(a) is respectfully requested.

VIII. CONCLUSION

In light of the above arguments, the Board is respectfully requested to review and overturn the rejections to claims 1-34 in connection with this application.

If the USPTO believes that personal communication will further the prosecution of this application, the Office is invited to contact Erin Hoffman, Reg. No. 57,752, at the telephone number below.

The Commissioner is authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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IX. CLAIMS APPENDIX

1. (PREVIOUSLY PRESENTED) A method of forming a nickel silicide layer on an exposed silicon surface comprising:

depositing a nickel alloy layer on the exposed silicon surface, the nickel alloy including nickel and an alloying metal that constitutes no more than about 10 atomic percent of the nickel alloy;

reacting the nickel alloy layer with the exposed silicon surface to form a nickel silicide layer having an upper layer and a lower layer, wherein the alloying metal is preferentially segregated in the upper layer.

2. (ORIGINAL) A method of forming a nickel silicide layer according to claim 1, wherein:

the lower layer includes at least 95 atomic percent nickel and silicon.

3. (ORIGINAL) A method of forming a nickel silicide layer according to claim 2, wherein:

the lower layer includes at least 99 atomic percent nickel and silicon.

4. (ORIGINAL) A method of forming a nickel silicide layer according to claim 3, wherein:

the nickel and silicon are present in the lower layer in an atomic ratio of about 1.

5. (ORIGINAL) A method of forming a nickel silicide layer according to claim 1, further comprising:

forming a capping layer on the nickel alloy layer before reacting the nickel alloy with the exposed silicon.

6. (PREVIOUSLY PRESENTED) A method of forming a nickel silicide layer according to claim 5, wherein: the capping layer includes a major portion of titanium nitride.

7. (PREVIOUSLY PRESENTED) A method of forming a nickel silicide layer according to claim 1, wherein: the alloying metal is at least one metal selected from a group consisting of tantalum, vanadium, zirconium, hafnium, tungsten, cobalt, platinum, chromium, palladium, niobium and combinations thereof.

8. (PREVIOUSLY PRESENTED) A method of forming a nickel silicide layer according to claim 1, wherein:

the alloying metal is tantalum and is present in a concentration of at least about 0.1 atomic percent of the nickel alloy.

9. (ORIGINAL) A method of forming a nickel silicide layer according to claim 8, wherein:

the nickel alloy consists essentially of nickel and tantalum, the tantalum being present in an amount between about 0.1 and about 5 atomic percent.

10. (ORIGINAL) A method of forming a nickel silicide layer according to claim 5, wherein: the capping layer has a nitrogen:titanium atomic ratio of at least about 0.5.

11. (ORIGINAL) A method of forming a nickel silicide layer according to claim 6, wherein: the lower layer has a first thickness; and

the upper layer has a second thickness, wherein the first thickness is at least 70% of a sum of the first thickness and the second thickness.

12. (ORIGINAL) A method of forming a nickel silicide layer according to claim 6, wherein: the lower layer has a first thickness; and

the upper layer has a second thickness, wherein the first thickness is at least 85% of a sum of the first thickness and the second thickness.

13. (ORIGINAL) A method of forming a nickel silicide layer according to claim 12, wherein: the lower layer has a tantalum concentration no greater than about 4.9 atomic percent; and

the upper layer has a tantalum concentration of at least about 5 atomic percent.

14. (ORIGINAL) A method of forming a nickel silicide layer according to claim 12, wherein: the lower layer has a tantalum concentration no greater than about 0.5 atomic percent; and

the upper layer has a tantalum concentration no greater than about 60 percent.

15. (PREVIOUSLY PRESENTED) A method of manufacturing a semiconductor device comprising:

defining an active region on a semiconductor substrate;

forming a gate electrode in the active region;

exposing a silicon surface on the semiconductor substrate;

forming a nickel alloy layer on the semiconductor substrate, the nickel alloy including nickel and an alloying metal that constitutes no more than about 10 atomic percent of the nickel alloy;

reacting a portion of the nickel alloy layer with the exposed silicon surface to form a nickel silicide region; and

removing an unreacted portion of nickel alloy layer from the semiconductor substrate;

wherein the nickel silicide region includes an upper layer and a lower layer, and further wherein the alloying metal is preferentially segregated into the upper layer.

16. (ORIGINAL) A method of manufacturing a semiconductor device according to claim 15, wherein:

nickel and silicon represent at least about 95 atomic percent of the lower layer of the nickel silicide region.

17. (ORIGINAL) A method of manufacturing a semiconductor device according to claim 16, wherein:

nickel and silicon represent at least about 99 atomic percent of the lower layer of the nickel silicide region.

18. (ORIGINAL) A method of manufacturing a semiconductor device according to claim 15, wherein:

the lower layer of the nickel silicide region includes nickel atoms and silicon atoms in a ratio of between about 9:10 and 10:9.

19. (ORIGINAL) A method of manufacturing a semiconductor device according to claim 15, further comprising:

forming a capping layer on the nickel alloy layer;

maintaining the capping layer until the nickel silicide region has been formed; and removing the capping layer.

20. (ORIGINAL) A method of manufacturing a semiconductor device according to claim 18, wherein:

the capping layer includes a major portion of TiN.

21. (ORIGINAL) A method of manufacturing a semiconductor device according to claim 15, wherein exposing the silicon surface on the semiconductor substrate includes:

exposing portions of the semiconductor substrate in a source/drain region formed in the active region.

22. (ORIGINAL) A method of manufacturing a semiconductor device according to claim 15, further comprising:

forming a gate capping layer on the gate electrode to protect an upper surface of a polysilicon layer included in the gate electrode.

23. (ORIGINAL) A method of manufacturing a semiconductor device according to claim 15, wherein exposing silicon surfaces on the semiconductor substrate includes:

exposing silicon surfaces only on the gate electrode.

24. (ORIGINAL) A method of manufacturing a semiconductor device according to claim 23, further comprising:

forming an insulating layer on the semiconductor substrate and the gate electrode; and

removing an upper portion of the insulating layer to expose a silicon surface on the gate electrode with a lower portion of the insulating layer covering source/drain regions formed in the active region.

25. (ORIGINAL) A method of manufacturing a semiconductor device according to claim 15, wherein exposing silicon surfaces on the semiconductor substrate includes:

exposing silicon surfaces in source/drain regions formed in the active region; and exposing a silicon surface on the gate electrode.

26. (PREVIOUSLY PRESENTED) A method of manufacturing a semiconductor device according to claim 15, wherein:

the alloying metal is at least one metal selected from a group consisting of tantalum, vanadium, zirconium, hafnium, tungsten, cobalt, platinum, chromium, palladium, niobium and combinations thereof.

27. (ORIGINAL) A method of manufacturing a semiconductor device according to claim 26, further comprising:

forming a capping layer on the nickel alloy layer;

maintaining the capping layer until the nickel silicide region has been formed; and

removing the capping layer.

28. (PREVIOUSLY PRESENTED) A method of manufacturing a semiconductor device according to claim 15, wherein:

the alloying metal consists essentially of tantalum.

29. (ORIGINAL) A method of manufacturing a semiconductor device according to claim 28, wherein:

tantalum constitutes no more than about 5 atomic percent of the nickel alloy.

30. (ORIGINAL) A method of manufacturing a semiconductor device according to claim 15, wherein reacting the nickel alloy with the exposed silicon surfaces to form nickel silicide regions on the semiconductor substrate includes:

heating the substrate and the nickel alloy layer to a temperature between about 250° C. and about 550° C. for a silicidation period of between about 10 seconds and about 30 minutes.

31. (ORIGINAL) A method of manufacturing a semiconductor device according to claim 15, further comprising:

completing the manufacture of the semiconductor device utilizing processes such that at least about 90 percent of the nickel silicide region remains nickel monosilicide, NiSi.

32. (ORIGINAL) A method of manufacturing a semiconductor device according to claim 31, wherein:

the nickel silicide region contains substantially no nickel disilicide, $NiSi_2$.

33. (ORIGINAL) A method of manufacturing a semiconductor device according to claim 15, wherein:

the lower layer has a first thickness;

the upper layer has a second thickness; and

the first thickness is at least 70% of a sum of the first thickness and the second thickness.

34. (ORIGINAL) A method of manufacturing a semiconductor device according to claim 15, wherein:

the lower layer has a first thickness;

the upper layer has a second thickness; and

the first thickness is at least 85% of a sum of the first thickness and the second thickness.

35-37. (CANCELED).

X. EVIDENCE APPENDIX

None.

XI. RELATED PROCEEDINGS APPENDIX

None.